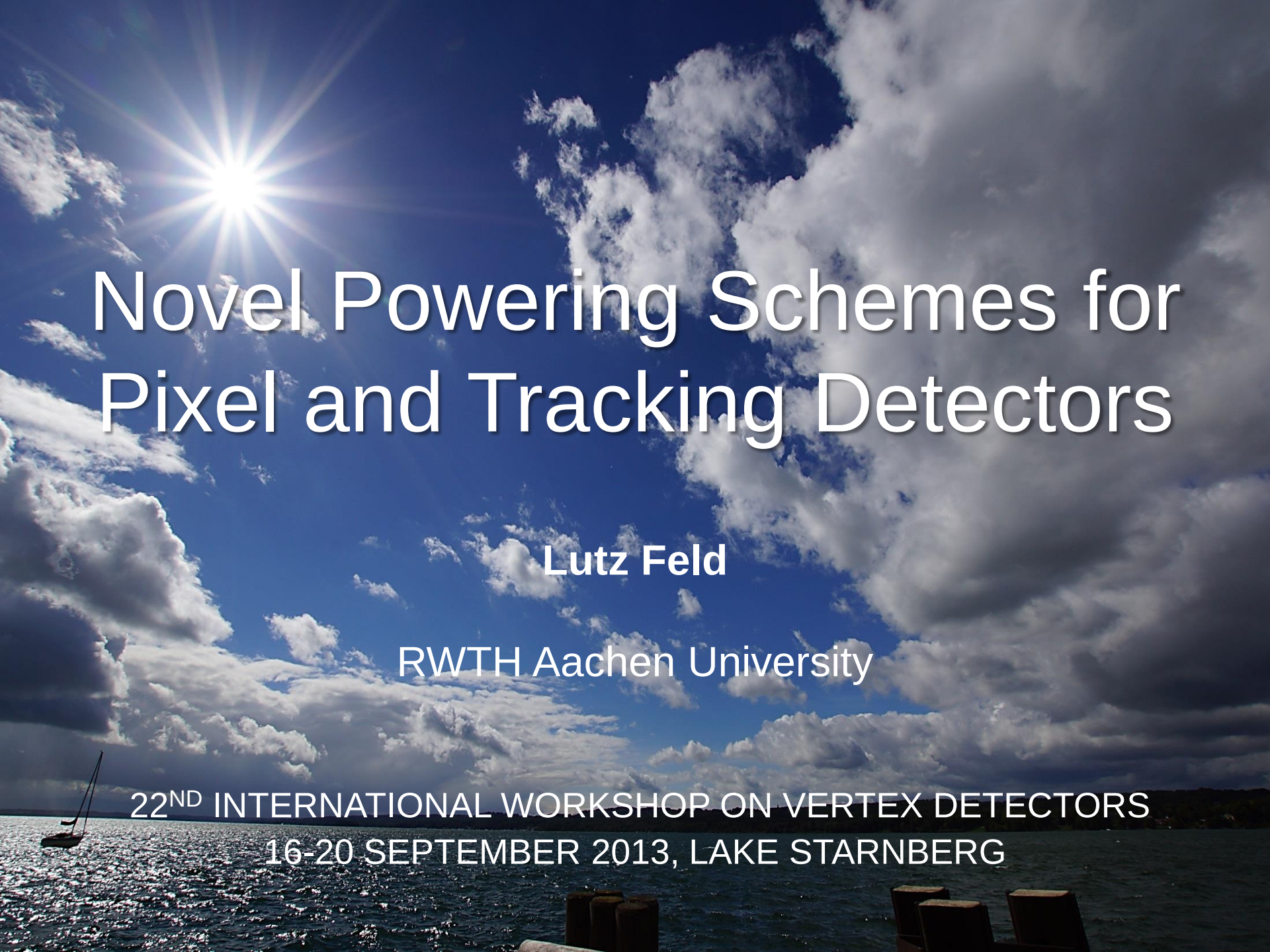

Novel Powering Schemes for Pixel and Tracking Detectors

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22ND INTERNATIONAL WORKSHOP ON VERTEX DETECTORS
16-20 SEPTEMBER 2013, LAKE STARNBERG

Outline

- The Power Challenge
- Powering Options
  - Serial Powering R&D
  - DC-DC Powering R&D

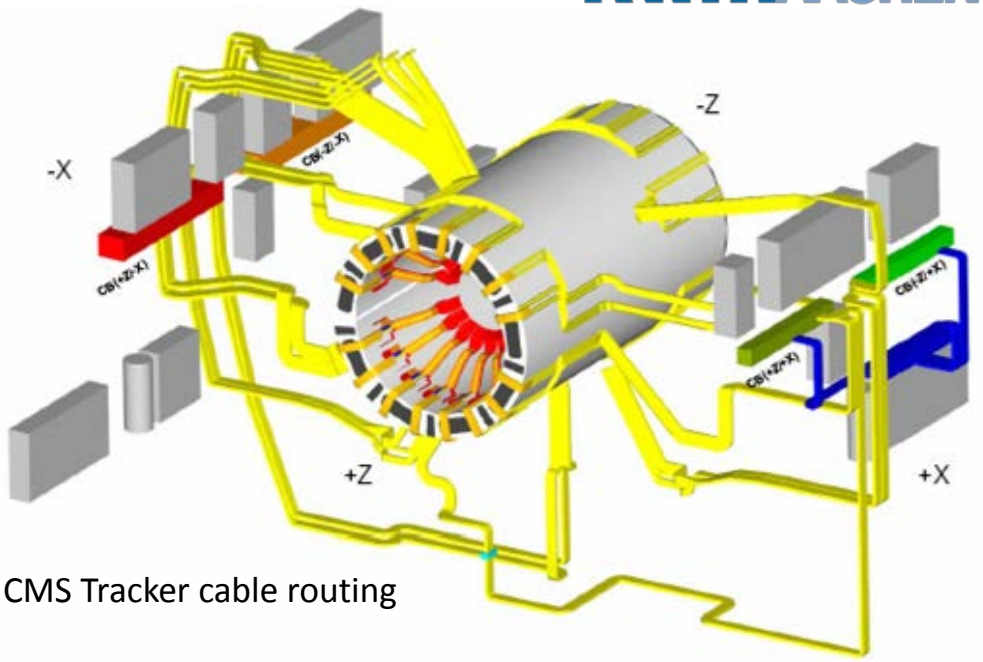
- Implementation of DC-DC powering into the CMS Pixel System
  - System design
  - System test results
- Summary

Powering today

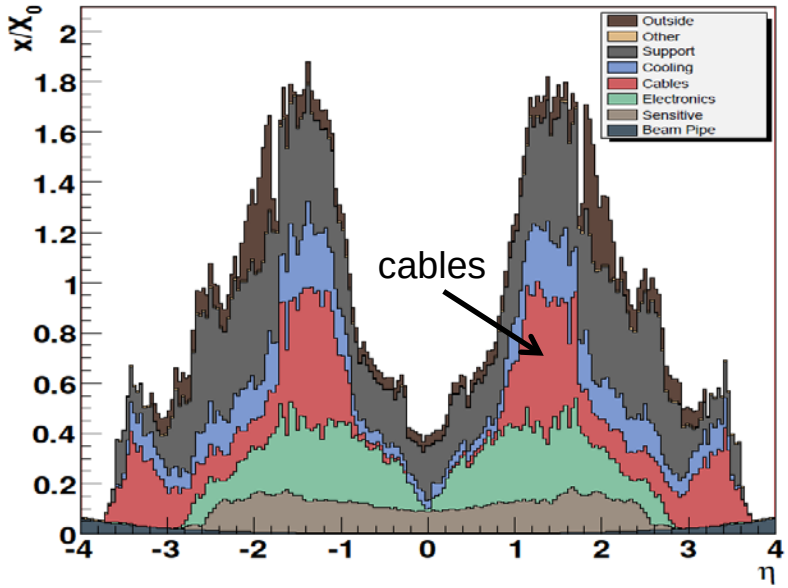
Example: CMS tracker

- ~15’000 modules in ~2000 power groups
- ASICs supplied at 2.5V and 1.25 V
- front-end power: 33 kW
- total current: 15 kA
- cable length ~50m
- loss in cables: 34 kW
- cable channels fully used
- 29 racks with up to 6 crates of power supply modules

50% power lost in cables



CMS Tracker cable routing



CMS Tracker material budget

The Power Challenge

- higher channel density
  - pattern recognition
  - resolution
- more functionality
  - hit correlation (triggering)
  - A/D conversion
  - sparsification
  - …
- higher speed
- technology scaling

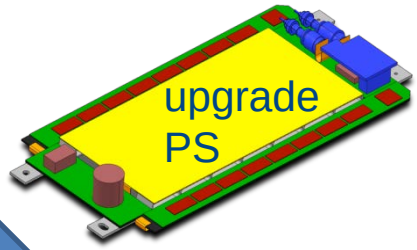
  250 nm → 130 nm → 65nm → …

  decreasing power per transistor

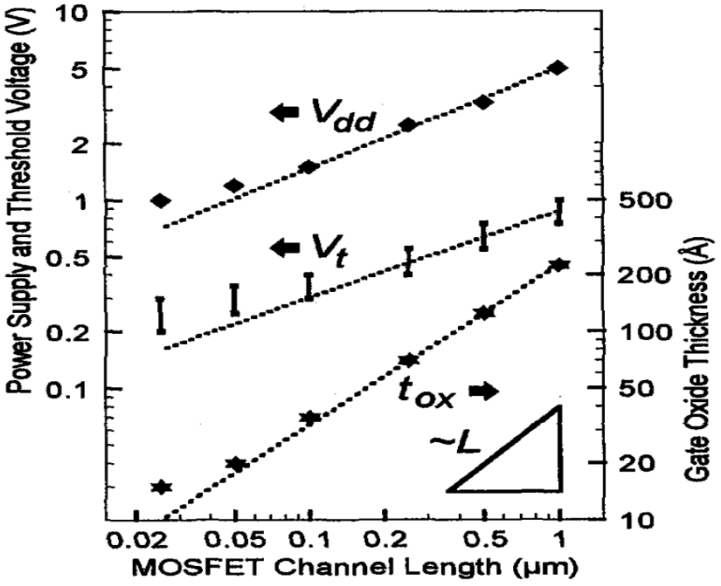
  2.5V → 1.5V → 0.9V → …

  decreasing voltage margins

6.1x11.7cm²
768+768 channels
P(FE-ASICs)=3.6W
50mW/cm²



4x10cm²
2000+33000 ch.
P(FE-ASICs)=4W
100 mW/cm²



[Y. Taur, *VLSI-TSA*, 1999]

Implications at the System Level

again CMS tracker as example:

- front-end power 35kW →70kW
- front-end supply voltage 2.5V → 1.25V

→ front-end current increases by factor 4

→ cable losses increase by **factor 16**

cannot increase conductor cross-section to compensate

should rather be reduced to improve material budget

need a novel powering scheme which

- is able to provide more power
- at a lower current
- with sufficient voltage control at modules
- with sufficient slow control features
- with sufficient fault tolerance
- with minimal extra material

Possible Solutions

1. add circuitry to each ASIC so that it can be supplied with 2.5V or higher
   - e.g. 2:1 charge pump
   - is widely used for CPUs
   - adds passive components next to each ASIC
   - switching noise may interfere with signal read-out

implemented in several ASICs (ATLAS FE-I4, CMS CBC, …) not covered in this talk

2. add circuitry so that a number of modules can be supplied with 2.5V or higher
   - e.g. DC-DC converter (charge pump or buck converter)
   - fewer components than in 1.
   - switching noise still an issue but further away from signal path

3. cascade modules
   - derive required voltages from the same current flowing through a chain of modules
   - rather different from today's powering scheme

Power Distribution Options

Conventional Powering

- well established
- excessive cable losses

P = U·I = (rU) ·(I/r)

→ supply power at higher voltage i.e. lower current

→ cable loss $P_{loss}=R \cdot I^2$ is reduced by factor r^2!

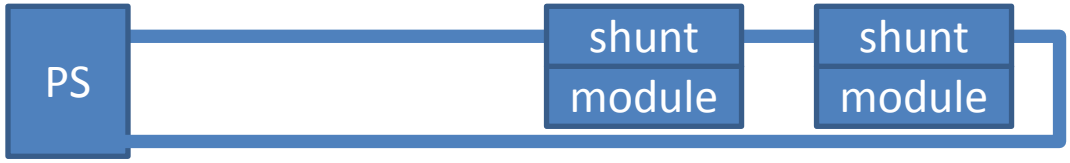
thinner and less cables

→ material budget reduction

DC-DC Powering r=conversion ratio

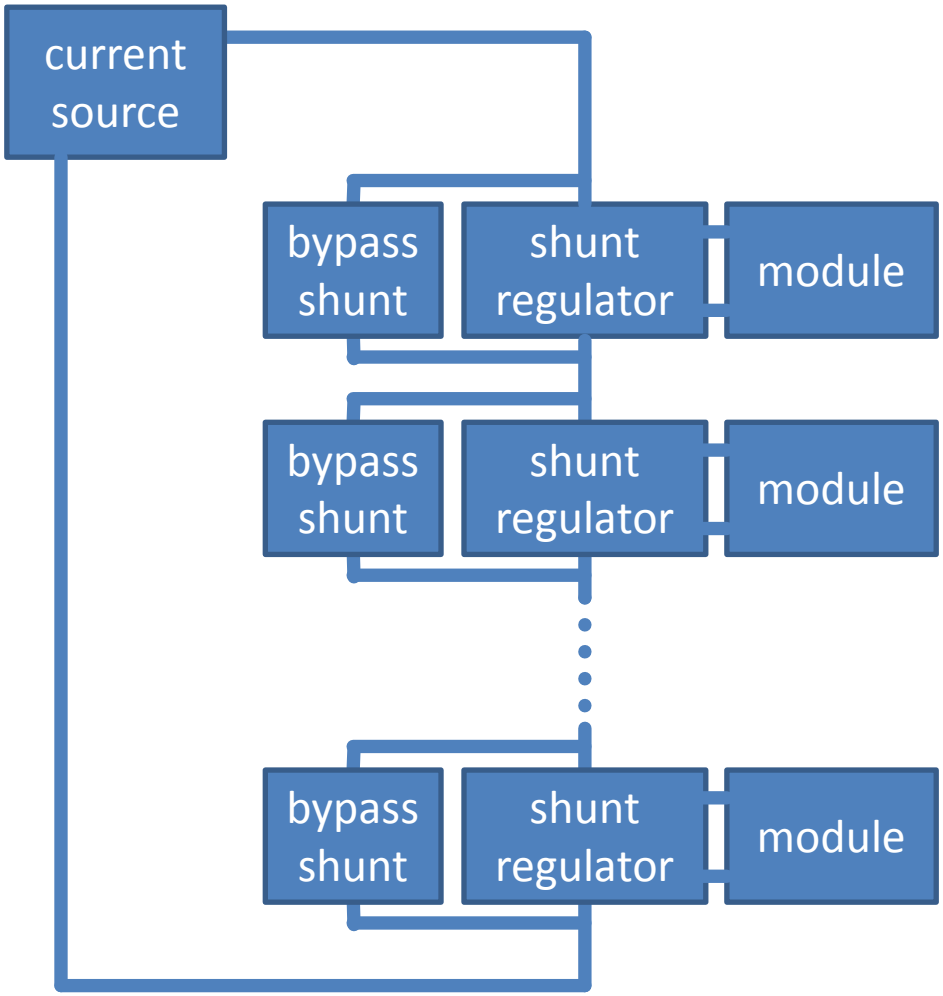
- system design is kept simple and close to current systems
- only one new component
- switching noise is a concern

Serial Powering r=number of modules in chain



- no switching
- each module has different ground potential
- modules in a chain are coupled, need safety features

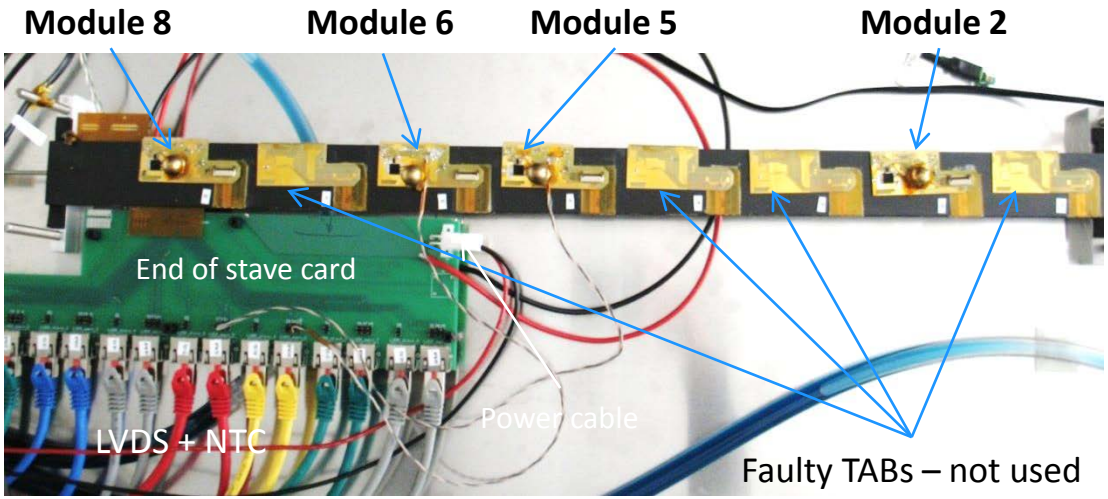
Serial Powering in more Detail

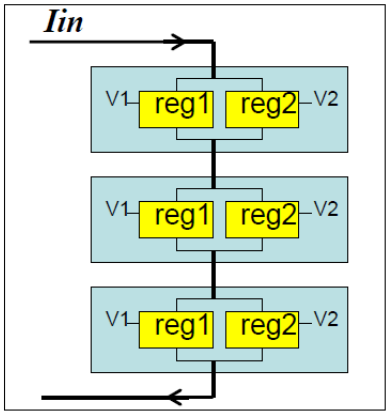


- current determined by biggest load in the chain
- load variations in a module can affect the whole chain
- read-out and control signals must be AC or opto coupled
- apart from this, additional components are small ICs
- with many modules in the chain the gain factor **r** can be quite high (e.g. 10-20)

Serial Powering: ATLAS Pixel

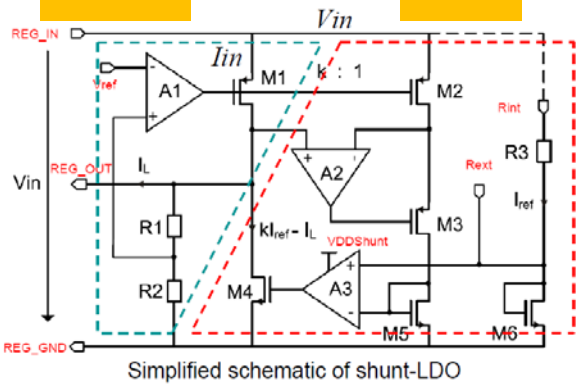
serial power chain of 4 modules on a stave





ShuLDOs can be operated in parallel
→ different voltages can be supplied

shunt LDO



Simplified schematic of shunt-LDO

Stability test: make module noisy by lowering the threshold

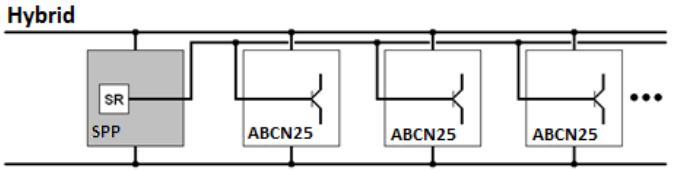
	Noise (e^-)			
Noisy module	**Module 8**	**Module 6**	**Module 5**	**Module 2**
No noisy module	131.2	145.1	144.6	130.8
Module 8	---	149.1 **4**	148.4 **3.8**	133.3 **2.5**
Module 6	134 **2.8**	--	147.4 **2.8**	134.2 **3.4**
Module 5	134.5 **3.3**	150 **4.9**	--	134.2 **3.4**

measured noise increase of max 5e^- on the other modules in the chain is not of concern

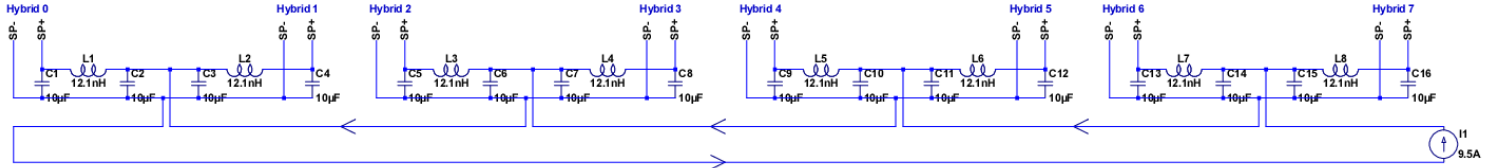
[thanks to Laura Gonella for the Bonn group]

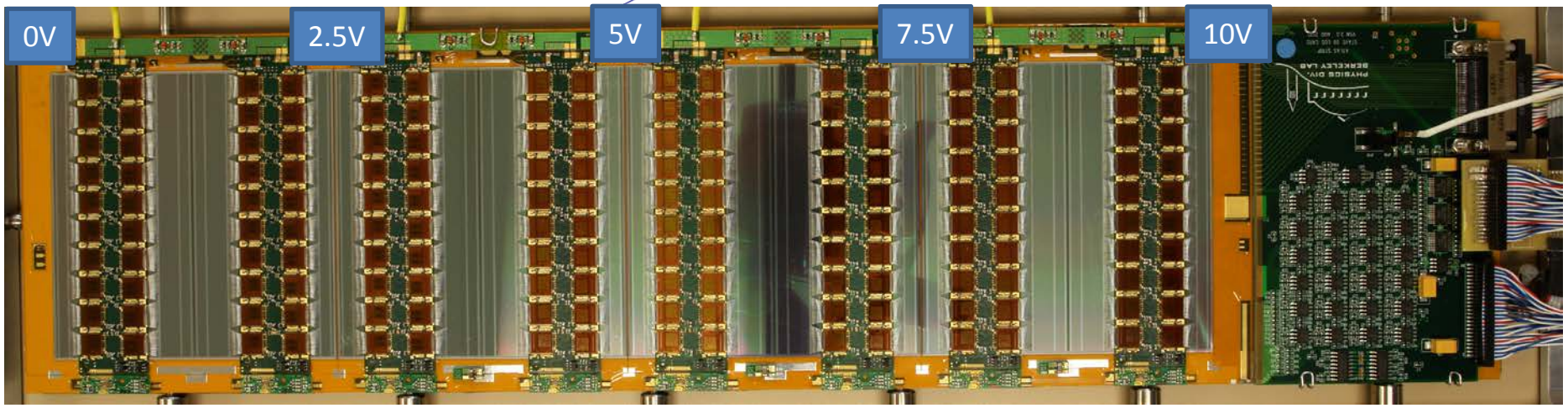
Serial Powering: ATLAS Strips

- Distributed SP Architecture
  - Shunt transistors within ABCN25 FE ASIC, 20 per hybrid
  - One control block per hybrid (SPP chip or commercial parts)
- Three short (8 hybrid) prototypes built
  - Some with protection circuitry (SPP chip commercial parts)
  - Good results in “Chain of Modules” Configuration
- Longer (24 hybrid) prototype to follow in the coming months
  - With integrated protection from SPP chip



Distributed SP Architecture (within the hybrid)





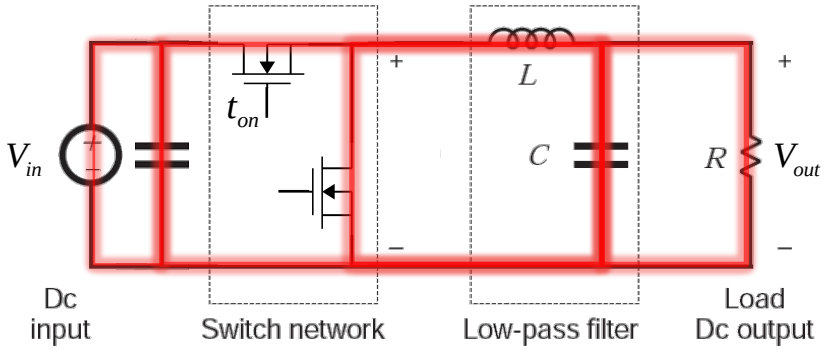
[thanks to Peter Phillips (RAL)]

DC-DC Powering: Buck Converters

operation principle

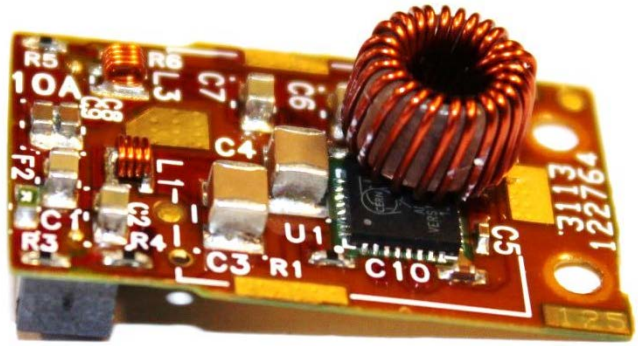
output voltage is regulated via feed-back loop by adjustment of duty cycle $D = \frac{t_{on}}{T}$:

$$\boxed{V_{out} = D \cdot V_{in}}$$ for lossless converter



main parameters

conversion ration	$r = \frac{V_{in}}{V_{out}} = 2...10$
switching frequency	$f = 1...4$ MHz
efficiency	$\eta = \frac{P_{out}}{P_{in}} = 60\ldots90\%$
current ripple at inductor	$\Delta I_L = \frac{V_{out}(1-D)}{L\ f}$



main loss mechanisms

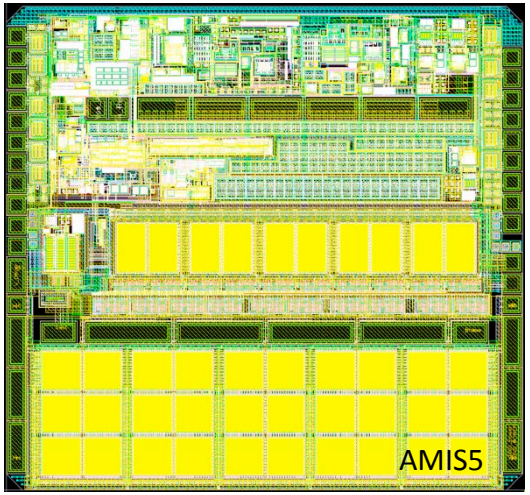
- resistive loss in inductor
- resistive loss in MOSFETs
- switching loss in MOSFETs $(\sim f)$
- driving loss in MOSFETs $(\sim f)$

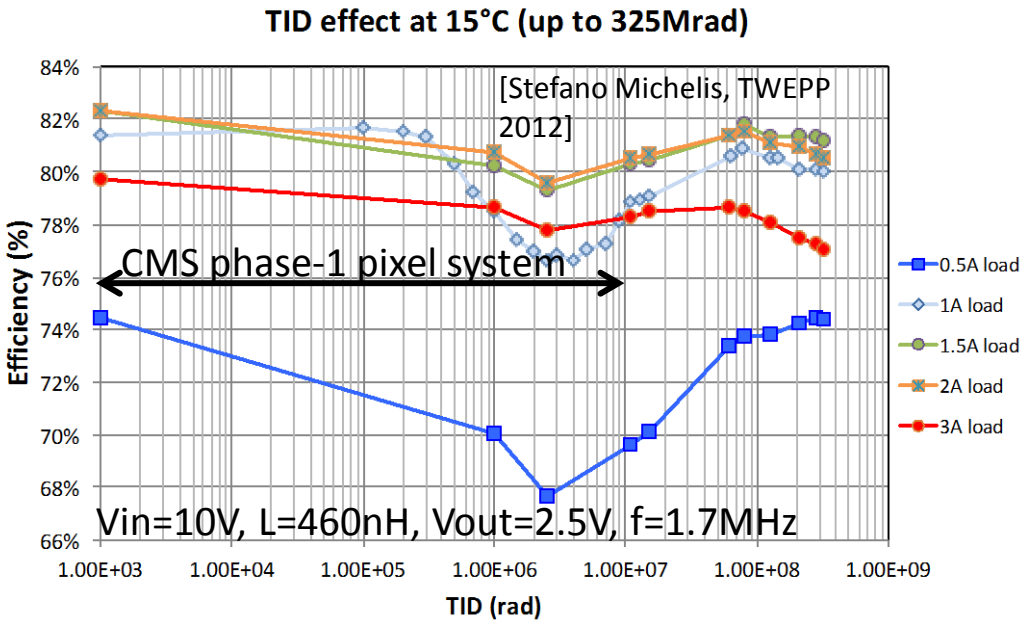
custom development necesssary

- radiation hard ASIC
- air core inductor for operation in magnetic field

Converter ASIC Development at CERN

- several iterations: **AMIS4/5, FEAST**
- developed by CERN-PH-ESE (St. Michelis, F. Faccio)
- radiation-tolerant design in AMIS I3T80 0.35µm CMOS technology (ON Semiconductor): TID above 200Mrad, displacement damage up to 7e14 1MeV neutrons/cm^2
- I_{out} < 3A, more is possible with proper cooling
- V_{in} < 12V
- f_s configurable from 1MHz to 3.5MHz
- V_{out} adjustable from 1.2V to 4V





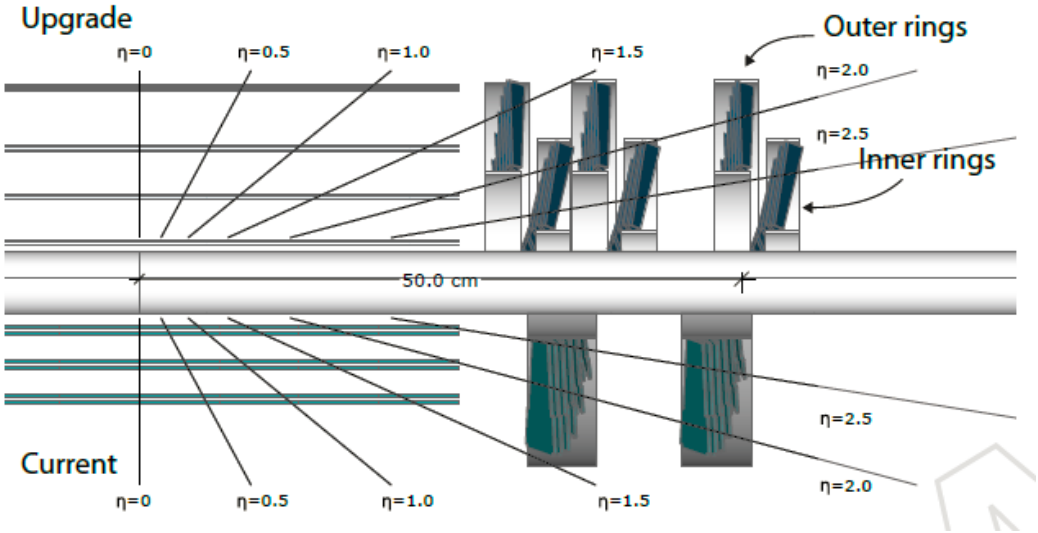
[2012 JINST 7 C01072]

CMS Pixel Upgrade

- current pixel detector specified for LHC design luminosity of $1 \cdot 10^{34}\,cm^{-2}s^{-1}$

- LHC planning: ~ $2 \cdot 10^{34}\,cm^{-2}s^{-1}$ between 2015 and 2018
  → pixel detector would have 50% dead time (at 50 ns bunch crossing interval)
  → **CMS plans to exchange pixel detector in shutdown 2016/17**

- **new pixel detector**
  - 4 barrel layers, 2x3 disks (now 3 layers, 2x2 disks)
  - new read-out ASIC
  - less material inside tracker acceptance
  - factor 1.9 more channels
  - → **factor 1.9 increase in power consumption**



- cable plant must be re-used: heat load would increase by factor 4

→ need a new powering scheme!

DC - DC for CMS pixel system

$V_{in} = 10\text{V}$

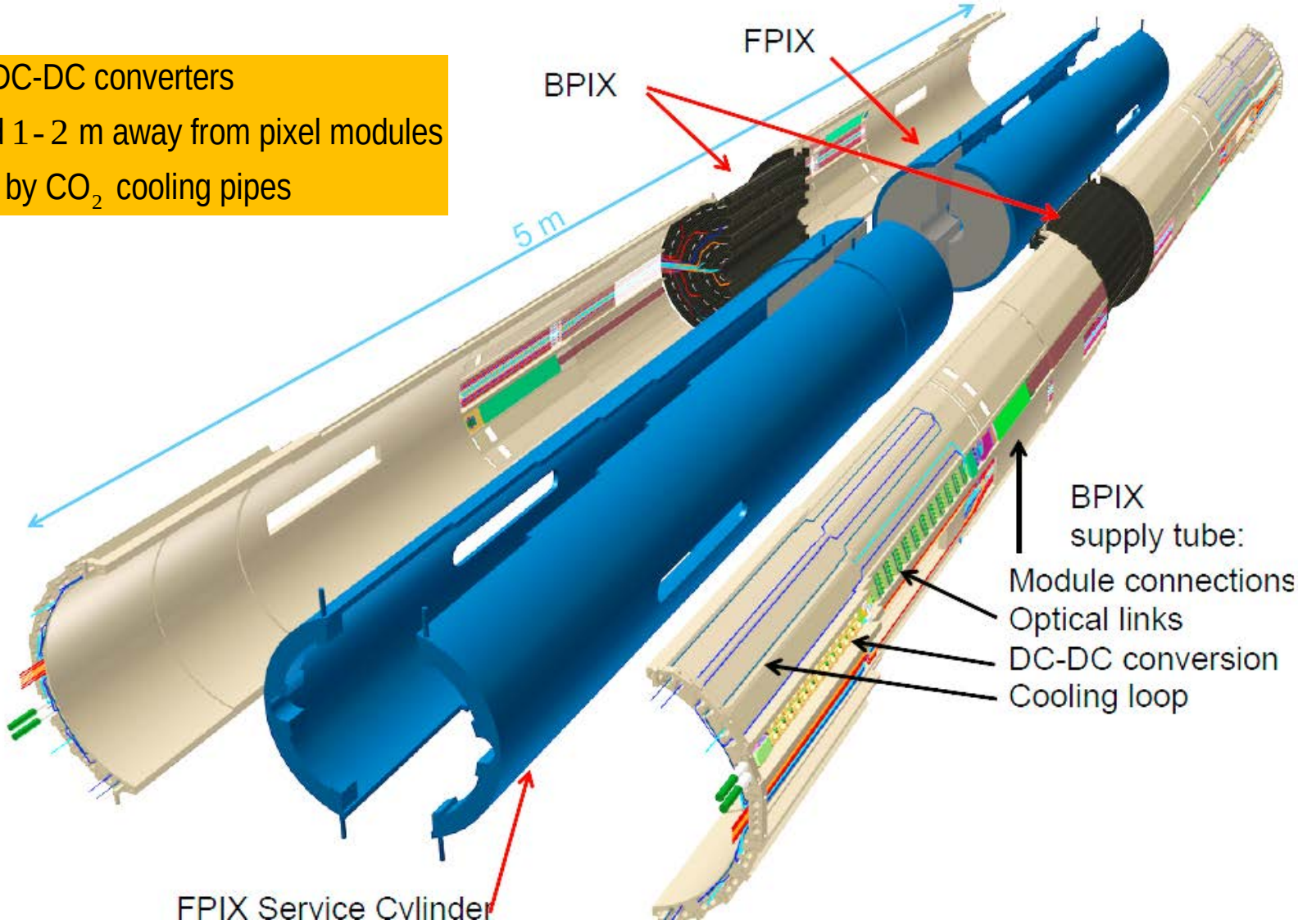
$V_{out} = 2.4\text{V or } 3.0\text{V}$

→ conversion ratio $3-4$

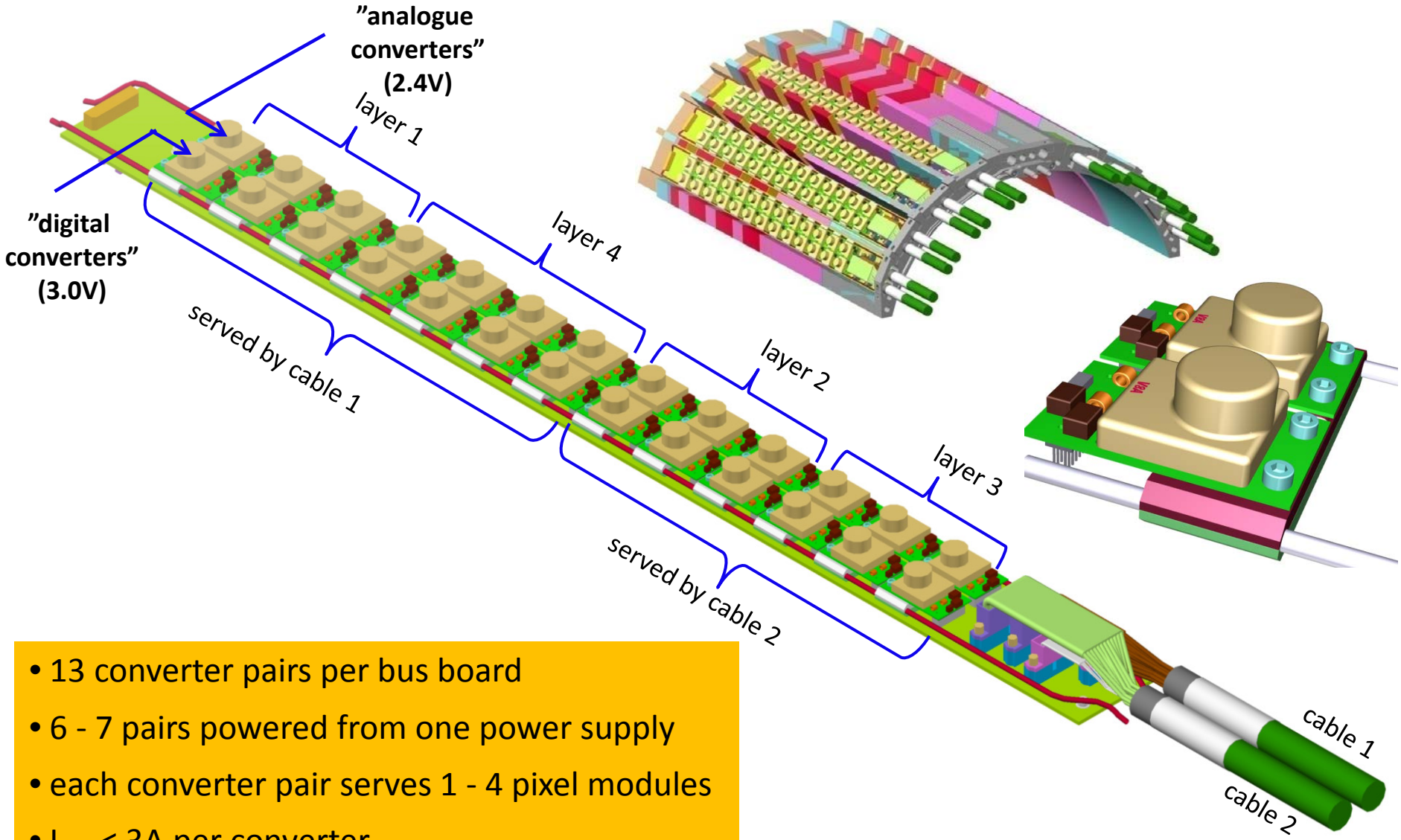
→ cable losses reduced by factor 10

Implementation into the CMS Pixel system

1184 DC-DC converters
located 1 - 2 m away from pixel modules
cooled by CO_2 cooling pipes



Implementation into the CMS Pixel system



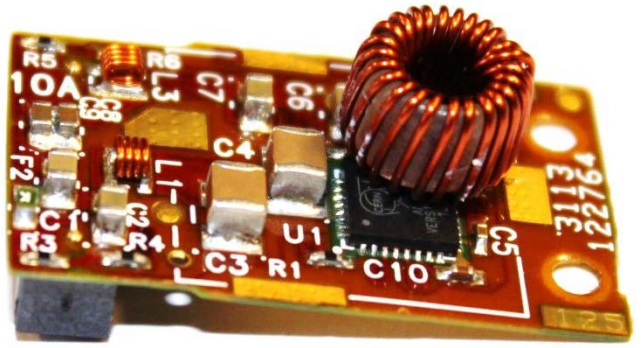
- 13 converter pairs per bus board
- 6 - 7 pairs powered from one power supply
- each converter pair serves 1 - 4 pixel modules
- I_{out} < 3A per converter

System integration issues

- DC-DC converters are a new component → no working experience
  → unclear which control and protection features are essential
  chosen approach:
  - converters switch off in case of over-temperature and under-voltage and switch back on when conditions are again fine, output current is limited
  - solid state fuse to disable converters with excessive current permanently
  - converters can be dis-/enabled and status is read via slow control communications
  - no remote sensing → voltage drops need careful attention
- no electromagnetic interference with pixel modules (and the rest of CMS)
- single event upsets in converter ASIC at some low level must be tolerated
- 'bus board' needed to distribute (large) currents to and from converters
- tight space constraints
- converters should be accessible/replaceable
- cooling needed (1-2W per converter)

DC-DC Converter Development

based on CERN ASICs AMIS4/5, and soon FEAST
V_{in} =10V
V_{out} = 3.0V or 2.4V
switching frequency f_s = 1.5MHz
2-layer PCB
pi-filters at in- and output

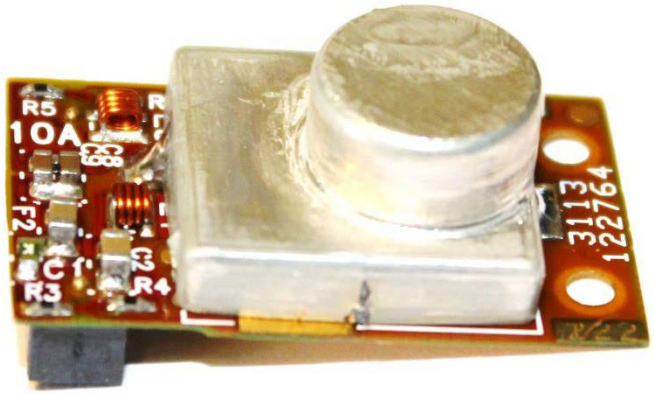


AC_PIX_V10 A with AMIS5: 2.8cm x 1.7cm

Toroidal plastic core **inductor** L = 450nH

Shield (0.3mm plastic with 30µm Cu + 1µm Sn) has 3 functions:

- shield magnetic emissions
- cooling contact for the coil
- segregation of “noisy“ parts from output filters

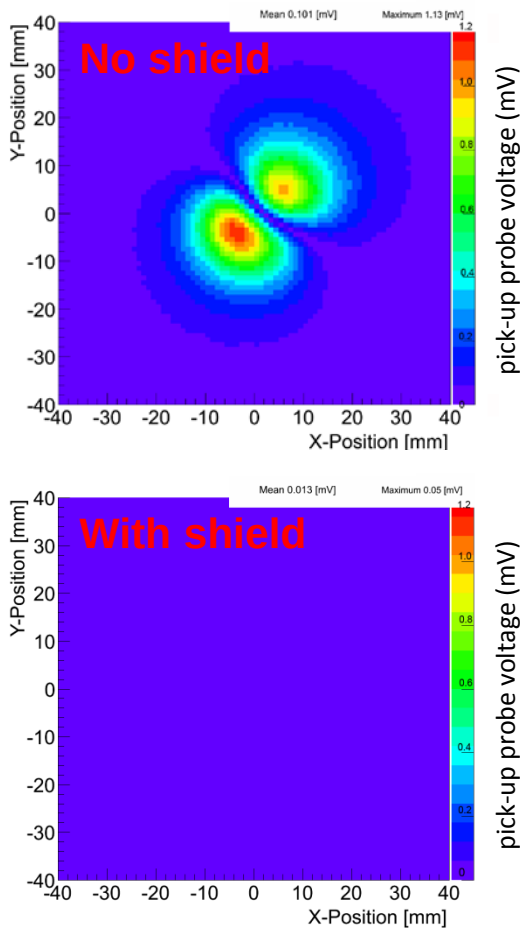


with shield; total weight ~3g

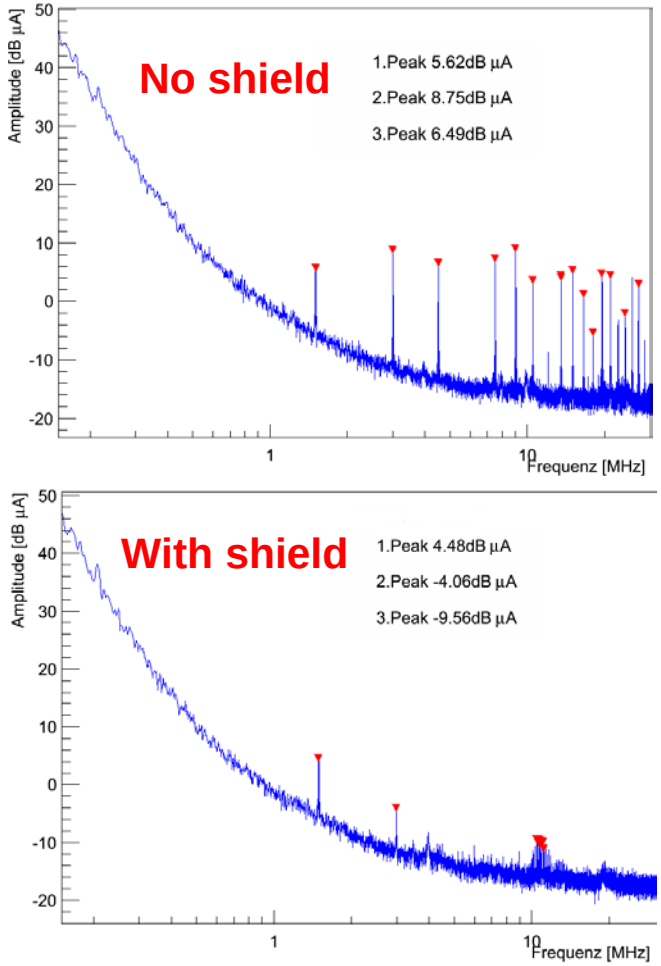
100 DC-DC converters have been built so far

Effectiveness of Shield

B-field, measured with pick-up probe above coil/shield

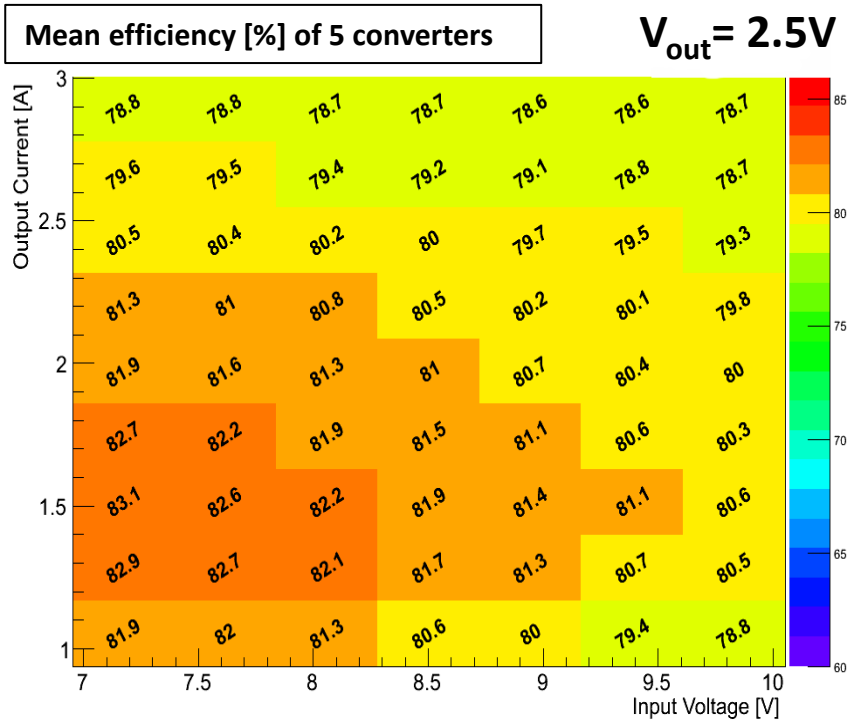


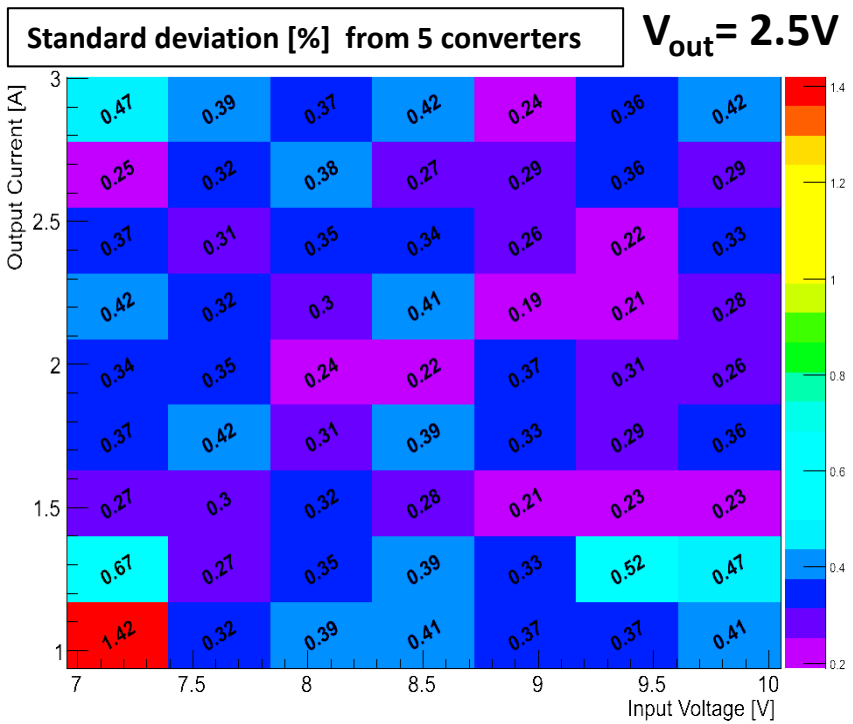
Common Mode output noise spectrum, measured with spectrum analyzer



Strong reduction of magnetic emissions and output noise

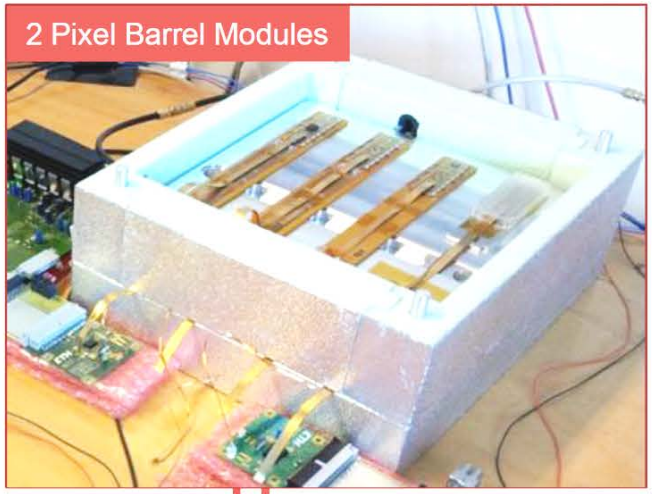
Efficiency





very good and uniform efficiency around 80%

System tests with 24 converters and 2 pixel modules

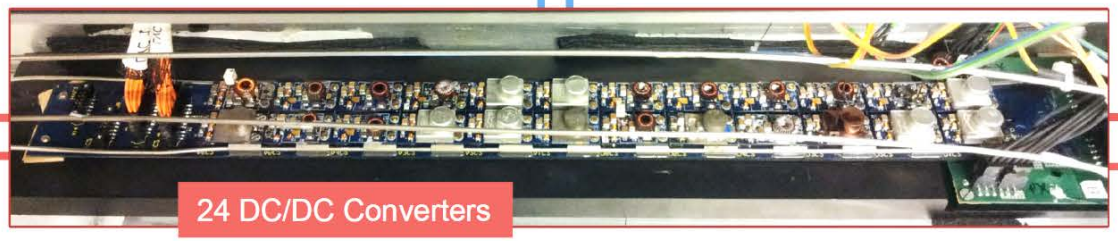


Electronic Load

(up to 24 x 3A)

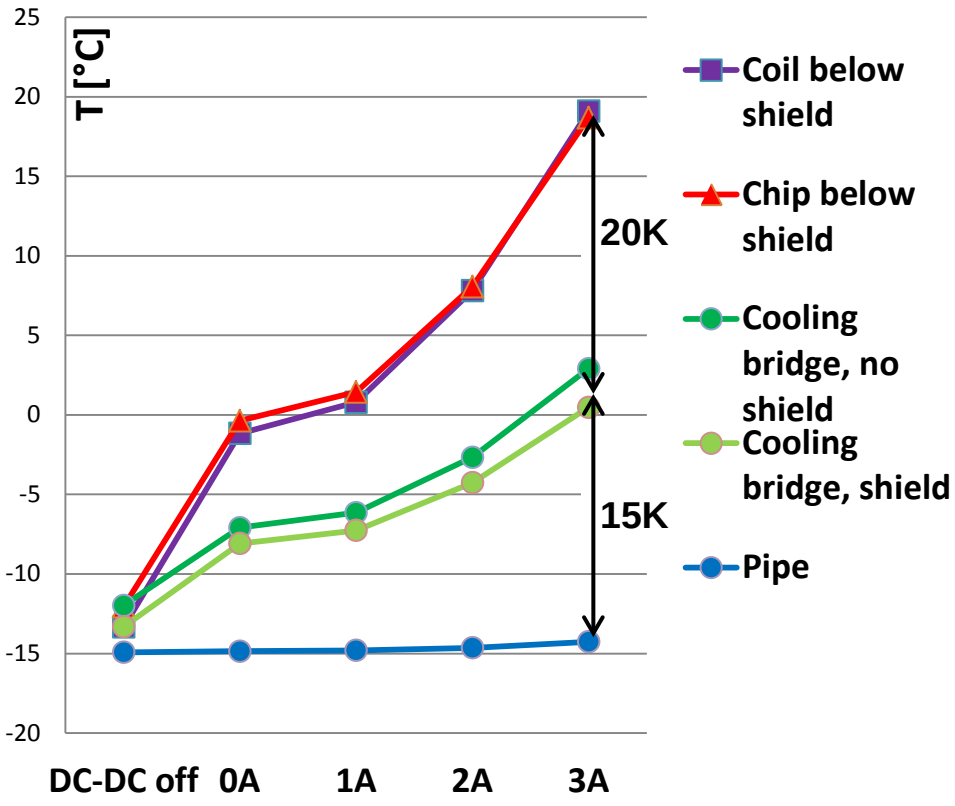
50m

2m

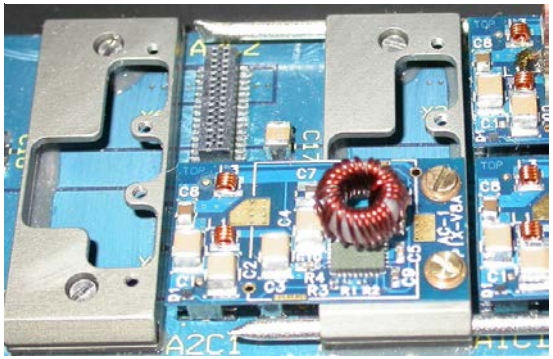


Cold Test

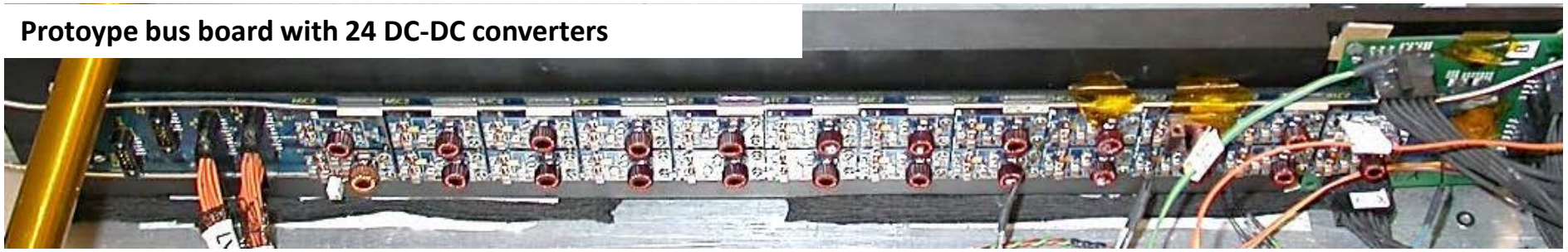
- two-phase CO_2 cooling system at -20°C
- fully equipped bus board (24 converters)
- pipes are thin: 1.7/2.0 mm in lab; 1.8/2.2mm in CMS
- programmable load can be applied to each converter



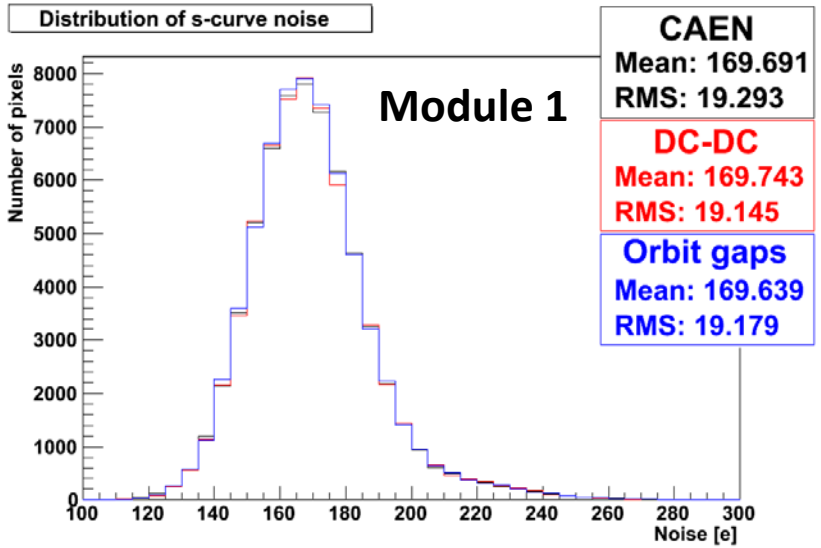
Aluminium cooling bridges

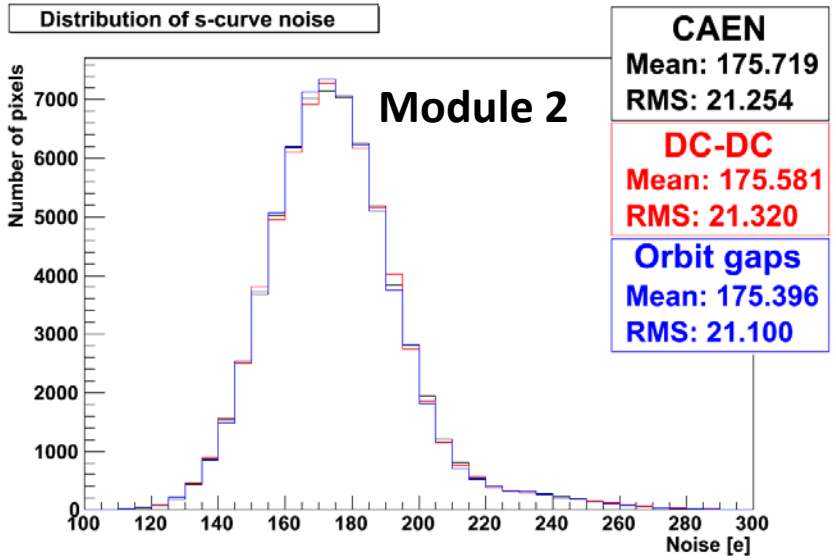


Protoype bus board with 24 DC-DC converters



Module noise with 24 converters running





Two pixel modules operated by standard power supply

a pair of converters with

24 converters operating in parallel

Load changes as expected from LHC orbit gaps

→ drop from 2A to 0A for 3µs every 89µs

DC-DC converters do not increase pixel module noise

Summary

- future pixel and strip tracking systems need improved powering schemes to cope with
  - increasing granularity
  - extended functionality
  - decreasing ASIC supply voltage
- different options available:
  - charge pump in each ASIC
  - DC-DC converters to power single or multiple modules
  - serial powering of modules
- all options have been shown to work in small systems (typically 4 modules)
- serial powering under study for ATLAS pixel and strips
- DC-DC powering under study for CMS pixel and strips, CMS HCAL, ATLAS strips, LHCb, Belle II, Panda
- system integration has to be carefully analyzed and studied and should guide the choice of an appropriate powering scheme
- DC-DC powering of CMS pixel detector described in detail as a case study